Full FPGA-Based Implementation of an Energy Efficient ONU with Cooperative Cyclic Sleep

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Abstract: A full FPGA-based implementation of an energy efficient ONU featuring cooperative cyclic sleep is presented. Evaluations show that the ONU successfully switches between states and maximal energy saving is achieved without violating delay requirements.

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1. Introduction

While many studies dealt with the issue of energy efficiency in Passive Optical Networks (PONs) by means of mathematical analysis or simulations [1,2], only few of them target experimental evaluation. For example, in [3], a partial implementation of an Optical Network Unit (ONU) featuring sleep mode is presented together with a testbed that considers only downstream transmission.

In this study, a full FPGA-based design of an energy efficient ONU featuring the cooperative sleep scheme [4,5] is presented. The ONU design is flexible in the sense that different sleep schemes can be embedded. The cooperative cyclic sleep (CCS) scheme, implemented and evaluated in this paper, controls dynamically not only sleep triggering (i.e., when and ONU is turned OFF) but also wake-up triggering (i.e., when an ONU is switched back ON), and adaptable ONU sleep time in order to maximize energy saving while guaranteeing frame delay requirements. Such decisions are based on OLT and ONU mutual consent by considering both downstream (DS) and US traffic load, frame delay constraint, and size and status of the finite data buffer.

2. Energy Efficient ONU Design and Cooperative Cyclic Sleep

2.1. FPGA Design of Energy Efficient ONU

Fig. 1 (a) shows the energy efficient ONU functional blocks. In the upstream direction, the Gen generates both data frames (Ethernet frames) and control messages (MAC control frames). Data frames are generated based upon the embedded traffic model whereas control message generation is triggered by the Sleep Ctrl. US data frames are forwarded to the Data FIFO whereas control messages are forwarded to the Msg FIFO. The Gen also provides the Sleep Ctrl with the estimated US traffic load. The Msg FIFO and the Data FIFO store US control messages and US data frames, respectively. The Msg FIFO has priority over the Data FIFO. The operation of the two FIFOs, i.e., storing or forwarding a frame/message, is controlled by the Sleep Ctrl finite state machine (FSM). The Data FIFO provides
the Sleep Ctrl with its occupancy level. Both data frames and control messages are sent to the Tx MAC and the Tx PHY for further processing before being transmitted.

In the downstream direction, the Rx PHY and the Rx MAC process the received frames and pass them to the Mon. Moreover, the PHY informs the Sleep Ctrl when it is ready for receiving/transmitting data from/to other blocks. The Mon checks incoming bit stream from the Rx MAC and informs the Sleep Ctrl when a DS control message is received. In case of control message reception, the Mon passes the control message content to the Sleep Ctrl. While the US transmission statistics are registered at the Gen, Msg FIFO, and Data FIFO, the DS statistics are registered at the Mon for purposes of result collection.

The Sleep Ctrl takes sleep-related decisions based on its current FSM state, i.e., ACTIVE, SLEEP, or POST SLEEP (see Fig. 1(b)) and on the inputs received from the other modules including the updated user delay constraint provided by the QoS Update module. In addition, the Sleep Ctrl triggers the on/off switching of the Tx and Rx PHY transceiver blocks accordingly to its FSM state. In the Sleep Ctrl, different sleep schemes can be implemented by simply customizing the FSM implementation.

The ONU design utilizes Altera 10GbE MAC and Altera 10GBASE-R PHY Intellectual Property (IP) cores that cover Tx MAC, Tx PHY, Rx MAC, Rx PHY in Fig. 1(a). In this paper, as the ONU transceiver is physically switched off during sleep state for saving energy, the PHY component is customized to include the power down functionality.

2.2. Cooperative Cyclic Sleep

The considered cooperative cyclic sleep scheme is illustrated in Fig. 1(b). The OLT starts a sleep period by sending a Request including an ONU sleep time when the OLT DS data buffer is empty. Then, it buffers DS traffic and waits for ONU’s feedback. If the ONU receives the Request when the ONU US data buffer is empty, it sends an ACK message, buffers US traffic, and switches off its transceiver. Otherwise, the ONU refuses to sleep by sending a NACK message and it remains active. If the OLT receives an ACK, it keeps buffering the DS traffic and waits the ONU to wake up.

The ONU can sleep for whole ONU sleep time or wake up during its sleep state in case the ONU US data buffer is almost-full, i.e., the available buffer space is not enough for US data coming during post-sleep time (i.e., \( T_{oh} \)). \( T_{oh} \) is the overhead time during which the ONU recovers clock and resynchronizes with network [5]. After waking up, the ONU transmits all US traffic in the buffer followed by a Confirm to ask for sleeping longer. Once the OLT receives the US traffic during ONU sleep states, it transmits DS traffic. If the OLT receives a Confirm when OLT DS data buffer is not empty, it sends a NACK asking the ONU to remain active. Otherwise, it sends another Request to the ONU.

To maximize energy saving while guaranteeing frame delay requirements, the sleep scheme chooses the maximal ONU sleep time as the minimum among four values computed during runtime: two buffer-based times, i.e., the maximum times the ONU and OLT can buffer US and DS traffic, respectively, without incurring frame loss given their estimated traffic load and buffer size; and two delay-based times, i.e., the maximum times the ONU can sleep so that the approximated US and DS frame delay are bounded by the corresponding constrained frame delay. The ONU provides the OLT with the US sleep-related parameters for computing the sleep time by means of US control messages.

3. Performance Evaluation

Energy saving \( \eta \) is computed based on the time the ONU sojourns in active and sleep states and the ratio of the ONU power consumption in sleep and active state:

\[
\eta = 1 - \frac{P_a T_a + P_s T_s}{P_a(T_a + T_s)} \leq \frac{(P_a - P_s)T_s}{P_a(T_{oh} + \text{RTT} + T_s)},
\]

where \( P_a \) and \( P_s \) are ONU power consumption in active and sleep state; \( T_a \) and \( T_s \) are the ONU time in active and sleep state, respectively. In Eq. (1), note that \( T_a \) includes also post-sleep time \( T_{oh} \) because the ONU is assumed to be fully powered in this period. In CCS scheme, the upper bound energy saving is achieved when \( T_a \) includes only \( T_{oh} \) and round trip time (RTT) (see Fig. 1(b)), namely there is no data in both transmission direction.

Fig. 2. (a) Testbed configuration; (b) An example of transition among ONU states.
To evaluate the effectiveness of the energy efficient ONU implementation and of the CCS scheme, an OLT featuring the protocol described in Fig. 1(b) has been implemented. The OLT and ONU are implemented on two Altera Stratix IV GT FPGAs as shown in Fig. 2(a) that are connected in electrical back-to-back configuration. For performance verification, the system is also implemented in Opnet modeler. US and DS data frames are generated with Poisson arrival process. Frame size is constant and set to 1250 bytes. Both DS and US data buffer size are set to 2 Mb. US data rate is fixed to 100 Mb/s whereas DS data rate is varied from 50 Mb/s to 625 Mb/s. Round trip time is negligible. Both DS and US maximum delay constraint are set to 10 ms. The power consumption ratio $P_a/P_s$ is assumed to be 10 \([5]\). Simulation and experimental results, in terms of average energy saving, frame loss rate, and frame delay, are reported together with the upper bound saving for comparison.

Fig. 2(b) shows an example of transition among ONU states in experiment as a snapshot captured from Altera debugging tool. As seen in the figure, the ONU successfully switches among the states based upon a request reception.

Both experimental and simulation results are within a relative confidence interval of 91\% with respect to the average values at the 95\% confidence level for all the metrics. Fig. 3(a) and (b) show that the experiment and simulation produce similar results. Furthermore, the obtained average saving approximates the upper bound value revealing that the CCS scheme could maximize the energy saving for the ONU. As seen in Fig. 3, when the DS rate increases, both obtained saving and experienced delays decrease. This is because the CCS sleep control dynamically adjusts sleep time to avoid frame loss. Indeed, a small frame loss rate (less than 0.6\%) is observed when the DS data rate is higher than 250 Mb/s. Fig. 3(b) shows that the DS and US average frame delay are always lower than the corresponding constrained delay.

4. Conclusion

This paper presented a flexible FPGA design of an energy efficient ONU featuring cooperative cyclic sleep (CCS) scheme. The results showed that the ONU successfully switches from active and sleep states saving maximal energy without violating the traffic average delay requirements given limited data buffers utilized at the OLT and ONU.

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